24. (New) A dynamic circuit having an evaluation phase, the dynamic circuit comprising:

a node;

a power rail;

at least one nMOSFET to conditionally pull the node LOW during the evaluation phase; and

a conditional keeper comprising

a logic gate having a first input port connected to the node and an output port; and

a first pMOSFET having a gate connected to the output port of the NAND gate, a drain connected to the node, and a source connected to the power rail.

A3 end

Remarks

Claims 1 - 24 are presently active, new claims 15 - 24 having been added by this Amendment.

In the office action dated 21 March 2002 ("Office Action"), the drawings were objected to; claim 1 was objected to because of an informality; and claims 1-14 were rejected under 35 U.S.C. §103(a) as being unpatentable over Allen et al., U.S. patent 6,002,292 ("Allen") in view of Arnold, U.S. patent 5,467,026 ("Arnold").

The various objections and rejections raised in the Office Action are addressed below.

Objections to the drawings

It is stated in the Office Action, top of page 2, that "The drawings are objected to because an open circuit at the gate of pMOSFET 208 is not shown in figure 2." Perhaps the Examiner meant that Fig. 2 does not show the gate of pMOSFET 208 connected to anything? Applicants' copy of Fig. 2 shows the gate of pMOSFET 208 connected to the

output port of inverter 206, which is connected to node 210. Without knowing the exact correction needed, Applicants are submitting a substituted Fig. 2 under a separate letter filed herewith. Applicants apologize if the Examiner received a poor copy of the drawings.

Objection to claim 1 because of an informality

Claim 1 is amended to correct an informality. A similar informality was found in claim 5, and it too has been amended.

35 U.S.C. §103(a) rejection of claims 1-14 over Allen in view of Arnold

Applicants respectively traverse the rejection of claims 1-14.

The rejection of claims 1-14 were based upon Fig. 4 of Allen and Fig. 1C of Arnold. We first discuss the relevance of Allen.

The circuit shown in Fig. 4 of Allen was discussed in the present application. This circuit appeared in Stasiak, et al., "A 2dn Generation 440ps SOI 64b Adder," ISSC 2000, pp. 288-289, which was included in an Information Disclosure Statement filed with the present application. Fig. 4 of Allen is identical to prior art Fig. 1 of the present application except for the order of the stacked pMOSFETs 112 and 114 in Fig. 1 (pMOSFETs 72 and 74 in Fig. 4 of Allen). The particular ordering of these pMOSFETs is immaterial. As discussed in the Background section of the present application, there are some disadvantages associated with the circuit of Allen. (See paragraph 0008 of the present application.)

Stacking pMOSFET 112 and 114 (pMOSFETs 72 and 74 of Allen) reduces their overall effective gain. To compensate for this reduced gain, the stacked pMOSFETs need to be sized up to approximately twice as large as compared to a single, non-stacked pMOSFET keeper. However, sizing up these pMOSFETs will use more chip area, and also increases the load on inverter 106 in Fig. 1 of the present application (inverter 68 in Fig. 4 of Allen). This increased load on inverter 106 may also degrade the response of pMOSFET 108 in Fig. 1 (pMOSFET 62 of Allen) when performing its standard keeper function during normal operating conditions unless inverter 106 is sized larger. However, sizing inverter 106 larger leads to a further increase in chip area, and also increases the

load on node 110 (node 58 of Allen). Increasing the load on node 110 may result in an increase in switching power and delay.

Embodiments of the present invention do not have the above discussed disadvantages associated with the circuit taught in Allen. Consider the circuit of Fig. 2 of the present application. There are no stacked pMOSFETs in either of the keepers. As a result, pMOSFET 220 need not be upsized. Furthermore, because microprocessors operate at a relatively low frequency during burn-in, NAND gate 218 may be sized relatively small. It is interesting to note that the circuit taught in Allen has 5 transistors making up the keeper. Namely, pMOSFETs 72, 74, 62, and the two MOSFETs used to synthesize inverter 68. The circuit of Fig. 2 in the present application has 8 transistors for the keeper functions. Namely, pMOSFETs 220 and 208, the four MOSFETs used to synthesize NAND gate 218, and the two MOSFETs used to synthesize inverter 206. Although the keeper functions of the circuit in Fig. 2 uses three more transistors than the circuit taught in Allen, it nevertheless uses less chip area and places a smaller load on node 210. In one particular simulation, it was found by the inventors that the circuit of Fig. 2 uses 62% less circuit area than the circuit taught by Allen, and presents a 30% smaller additional load on the node.

The above results and discussion were presented in a peer-reviewed paper presented by the inventors, "A Burn-In Tolerant Dynamic Circuit Technique," A. Alvandpour et al., IEEE CICC '02, Orlando Florida. For the convenience of the Examiner, a copy of the paper is provided as Exhibit A attached at the end of this Office Response. Because the publication date is well after the filing date of this Application, it has no bearing on the patentability of this Application.

Nowhere does Allen teach or suggest the circuit of Fig. 1. Indeed, the present patent application teaches that there are some disadvantages with the circuit of Allen, and proposes a novel circuit to address these disadvantages.

Referring now to Fig. 1c of Arnold, it should be noted that this is a pseudo-nMOS circuit. Under normal operating conditions, the test signal is HIGH, in which case pMOSFET 106 is always ON. During testing, the test signal is LOW, so that NOR gate 112 acts as an inverter with respect to the output of the circuit, in which case pMOSFET 106 will be ON when the output voltage V_{OUT} (110) is HIGH and OFF when the output

voltage V_{OUT} is LOW. Thus, during testing, the combination of NOR gate 112 and pMOSFET 106 act as a conventional keeper.

Arnold does not teach or suggest anything about burn-in conditional keepers. Therefore, in light of the above discussion regarding Allen and Arnold, Applicants believe that these references, taken either separately or in combination, do not suggest or motivate the novel circuit of Fig. 1.

The above discussion has been with respect to the embodiment circuit of Fig. 1. The Applicants now address the patentability of the claims.

Claim 1 includes the limitation of a NAND gate connected to the first pMOSFET, where the NAND gate has an input port connected to the node of the dynamic circuit. As discussed above regarding the circuit of Fig. 1, using a NAND gate actually adds more transistors than the circuit taught in Allen, but the inventors have found that the actual circuit area is decreased, and there is less loading of the node.

Therefore, Applicants believe that there is no motivation or suggestion, upon reading Allen and/or Arnold, to construct a circuit using a NAND gate as recited in claim 1, and therefore, claim 1, and claims 2-4 by virtue of their dependency upon claim 1, are believed patentable over the cited references.

The above discussion regarding the patentability of claim 1 also applies to claim 5, and to claims 6-7 which depend upon claim 5.

Claim 8 recites the limitation that the "first transistor and the logic gate provide a keeper function to the node if and only if the second input port of the logic gate is at a voltage indicative of the dynamic circuit being in the burn-in condition." Note that in the circuit of Allen, pMOSFET 74 and inverter 68 do not provide a keeper function during burn-in unless pMOSFET 72 is also ON. Thus, the "if and only" condition of the claim language is not satisfied by the circuit of Allen.

Consequently, Applicants believe that claim 8 and dependent claims 9-14 are patentable over the cited references.

Patentability of new claims

New claims 15-24 have been added. These claims add the additional limitation that the first pMOSFET (or first transistor) is connected to the power rail, or provides a

low impedance path to the power rail when ON. This limitation further distinguishes these claims from the cited references, because pMOSFET 74 of Allen is not connected to the power rail, and does not provide a low impedance path to the power rail when ON because pMOSFET 72 also needs to be ON.

Respectfully submitted,

Seth Z. Kalson Dated: 7-16-02

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Reg. no. 40,670
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Version of Amended Claims Showing Changes

1. (Amended) A dynamic circuit having an evaluation phase, the dynamic circuit comprising:

a node;

at least one [nMOSFETs] nMOSFET to conditionally pull the node LOW during the evaluation phase; and

a conditional keeper comprising

a NAND gate having a first input port connected to the node and an output port; and

a first pMOSFET having a gate connected to the output port of the NAND gate and having a drain connected to the node.

5. (Amended) A dynamic circuit comprising:

a node having a voltage;

a pullup transistor to pull the node HIGH;

a network comprising at least one [transistors] transistor to conditionally pull the node LOW if the pullup transistor is OFF;

a NAND gate having a first input port responsive to the node voltage, having an output port with a voltage, and having a second input port; and

a first transistor responsive to the output port voltage of the NAND gate to pull the node HIGH only if the second input port of the NAND gate is HIGH.

Exhibit A

A Burn-In Tolerant Dynamic Circuit Technique

A. Alvandpour [1], R. Krishnamurthy [1], S. Borkar [1], A. Rahman [2], C. Webb [2]
Microprocessor Research, Intel Labs [1], Portland Technology Development [2]
Intel Corporation, Hillsboro, Oregon, 97124 U.S.A.

Abstract

Time, cost and efficiency of burn-in test are severely impacted by the required functionality of leaky sub-130nm dynamic circuits during the burn-in. In this paper, we present an efficient keeper technique, which is active during the burn-in, and inactive at normal operating condition. As a consequence, dynamic circuits remain functional at burn-in, without relaxing the maximum burn-in condition, and without any significant performance degradation at normal operating conditions. Compared to the conventional technique, and at the same level of burn-in robustness, up to 17% higher performance has been observed at normal operating condition across 2-to-6 ways dynamic gates in a projected 100nm technology.

Introduction

"Burn-in" or stress test ensures high reliability for advanced microprocessors [1]. During the burn-in, functionality of circuits are monitored under extreme operating condition, where both temperature and supply voltage may exceed the normal operating range (up to 40%). The elevated temperature and voltage accelerate the time to early-failures (Fig.1), which are dominantly due to manufacturing defects. Subsequently, the units with early failures are identified and removed.

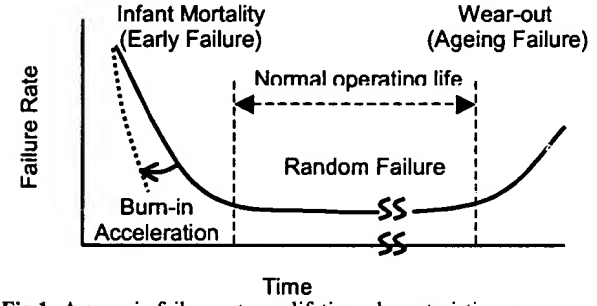

Fig.1: A generic failure rate vs. lifetime characteristic curve.

Each single unit has to pass the test (between 2-24 hours) and thus burn-in is a time consuming and relatively expensive process, suggesting that the early failures have to be accelerated as much as possible [1-3]. The failure-acceleration increases strongly with higher temperature and voltage, and can be expressed [1] as:

$$A_F = e^{[E_a/K_b\,(1/T_o - 1/T_{BI})]} \cdot e^{[C\,(V_{BI}-V_o)]}$$

Where, A_F is the time acceleration factor, [T_{BI}, V_{BI}], and [T_o, V_o] are burn-in and reference temperatures and voltages respectively, E_a is the activation energy, and C is a voltage acceleration constant.

Thus, in order to reduce the burn-in time and cost, it is highly desirable to provide the maximum burn-in temperature and voltage levels ultimately bounded by process reliability considerations only.

During the burn-in, leaky sub-130nm dynamic circuits are required to remain functional [4]. However, the elevated temperature and voltage increase the leakage currents exponentially (Fig. 2-3). The large leakage currents can discharge the dynamic nodes, resulting in incorrect operation of dynamic circuits. As a consequence:

- The burn-in condition has to be relaxed, resulting in a poor burn-in and/or a longer burn-in time with a significant increase in burn-in cost.
- Or, standard keepers (PK_0 in Fig. 4) have to be sized for burn-in and thus oversized for normal operating condition with attendant degradation of microprocessor performance.

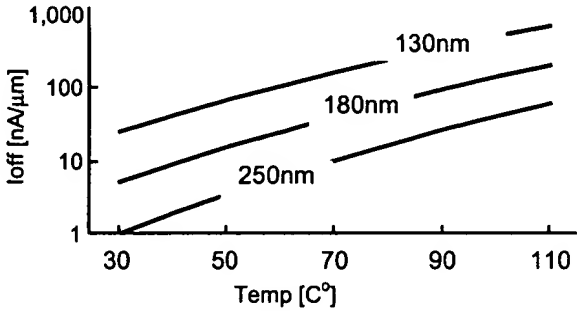

Fig.2: MOSFET leakage current versus temperature and technology scaling.

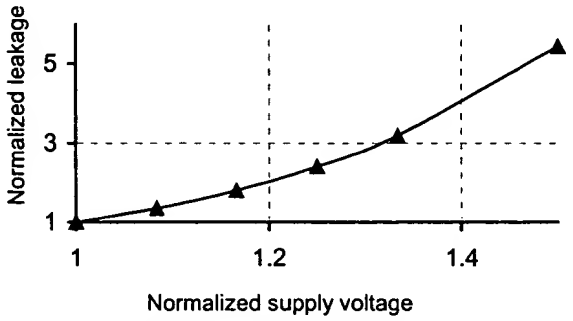

Fig.3: Leakage current vs. supply voltage for a static CMOS inverter in a 130nm technology. Normalized at the normal operating level.

In this paper, we present an efficient conditional burn-in keeper, which is a modified version of [6, 7] aimed for burn-in functionality of sub-130nm dynamic circuits. The burn-in conditional keeper allows the maximum burn-in stress condition, without any significant impact on delay of the dynamic circuits at normal operating condition.

Further, compared to the previously presented burn-in keeper circuit in [8], the proposed keeper requires 60% smaller transistor area, and contributes to a 30% smaller extra load at the output of the dynamic gates.

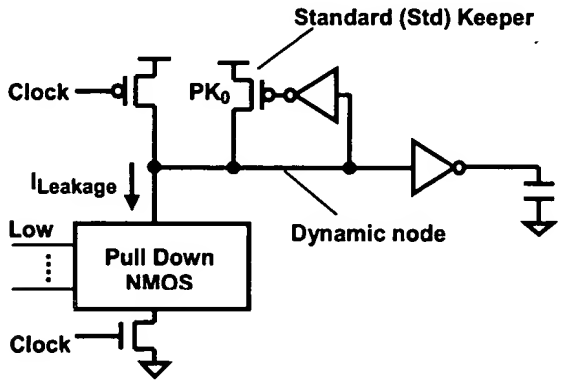

Fig.4: A dynamic gate with the conventional keeper.

Circuit Description

Fig. 5 shows a dynamic gate with the proposed burn-in conditional keeper, *BI-CKP*. The additional keeper-strength is provided by the transistor PK_B, which is activated by a burn-in signal *BI*='1'. In burn-in, the *NAND* gate acts as an inverter, and the effective channel width of the keeper is $W_{BI\text{-}CKP}$ = W(PK_1)+W(PK_B). When switching from burn-in mode to the normal mode, the only action needed is to deactivate the PK_B by the burn-in signal, *BI*='0', where PK_1 remains the only active keeper.

During the burn-in, microprocessors are operating at a relatively low frequency, and the performance of the gates is not an issue as long as they are functional. As a consequence, the burn-in keeper, PK_B, can be sufficiently large to maintain the robustness of dynamic circuits, without any significant impact on the performance of the circuits under normal operating condition. Further, the relaxed speed requirement allows the *NAND* gate to utilize minimum size devices, and therefore occupies a small area and a minimum additional load on the output of the dynamic gates.

Fig. 6 shows a similar keeper technique used in [8]. The main difference between the burn-in keeper in [8] and our burn-in keeper is the topology of the keeper circuits. In [8], the stacked p-transistors, PK_{X1}, and PK_{X2} together comprise the burn-in keeper, which is conditioned by an activation signal, *BI#*. Compared to the DC gain of the single transistor PK_B in Fig. 5, the PK_{X1}, and PK_{X2} must be upsized to about 2X larger in order to compensate for the impact of the stack-effect.

This results in ~4X larger effective pull-up keeper. Further in [8] an inverter is used to drive both the normal keeper and the potentially large burn-in keeper PK_{X2}. The resulting increase in inverter size propagates to the load on the output of the actual dynamic gate.

Thus, in spite of the fact that the burn-in keeper in [8] has a fewer number of transistors, however, the proposed burn-in keeper consumes significantly smaller transistor area, and contributes to a smaller additional load at the outputs of dynamic gates.

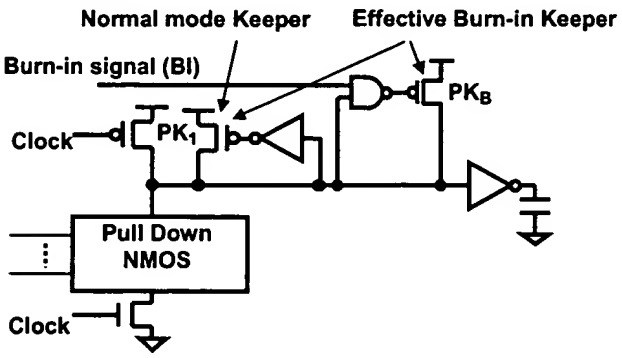

Fig.5: A dynamic gate with the proposed burn-in conditional keeper circuit. PK_B is unconditionally off at normal operating condition.

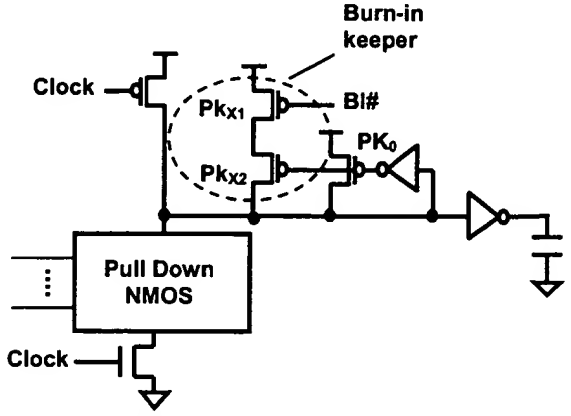

Fig. 6: Previous work; burn-in keeper in [8].

Performance, Robustness Comparisons

In this section, we present simulation results for three 4-stage domino circuits in Fig. 7, where the pre-charged gates are 2, 4, or 6 input dynamic NORs, each followed by a static inverter. Buffers are inserted for realistic edge-rate of clock and input signals to the first stage. For other stages, each input-signal is driven by a separate NOR gate from the previous stage. A Lagrange-Multiplier based quadratic optimizer has been used to size all transistors optimally, and the p/n ratio for the static inverters is designed to ensure the maximum DC-noise margin. The circuits utilize low-Vt devices from a dual-Vt 100nm technology, projected from the 130nm technology in [5].

The standard (Std) keepers (PK_0, in Fig. 4) were initially sized for the worst-case leakage process corner at normal operating condition. The worst-case leakage corner provides devices with highest leakage currents due to the potential worst-case process variations.

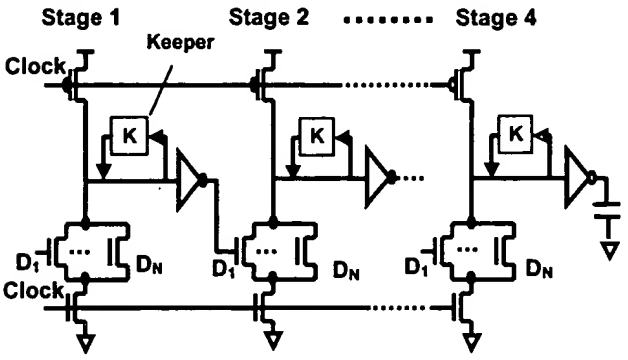

Fig. 7: Test circuit; a 4-stage domino circuit with dynamic N-input NOR gates, where N can be 2, 4, or 6.

To ensure a uniform sizing-methodology, the keepers channel widths were sized as a percentage of the effective worst-case (largest) channel width of the pull-down network. Hence, keepers sized with a certain percentage of the effective pull-down result in the same level of robustness, independent of the topology and fan-in of the pull-down network. However, it is important to note that the impact of keeper upsizing on delay depends strongly on the topology of the network, and is determined by the weakest pull-down path.

Fig. 8 shows the output voltages (1^{st}-to-4^{th}) of the 6-input conventional dynamic *NOR*s in the 4-stage domino circuit in Fig. 7. The figure shows the case, where the gates are in evaluation phase (clock High) and the pre-charged outputs should remain High. Since the standard keepers are sized for normal operating condition (nominal supply voltage, Vcc), all the gates show the same output voltage drop (due to worst-case leakage) indicating that the noise has not been propagated from one dynamic stage to the next stage. Thus, the domino circuit is functional and stable at worst-case normal operating condition.

Fig. 8 also shows the same circuit at burn-in (1.4Vcc). Where, the dynamic output nodes of the four stages are marked as BI[1^{st}]-to-[4^{th}]. The figure shows that the circuit operates incorrectly at burn-in. The noise generated by the large leakage currents exceeds the unity gain noise margin of a domino stage ({output noise/input noise}>1). Thus the noise propagates and increases through each stage, resulting in a functional failure at the third stage in this example.

Fig. 9 shows, that 2X larger standard keeper can maintain the functionality of the domino circuit at burn-in. The same waveforms show the case, where dynamic gates utilize *BI-CKP*, with an unchanged normal mode keeper, PK_1, where: $W(PK_1)=W(PK_B)=0.5W(PK_0)$.

Thus at burn-in, the domino circuit with the *BI-CKP* results in the same robustness (and performance) as that with 2X oversized standard keepers.

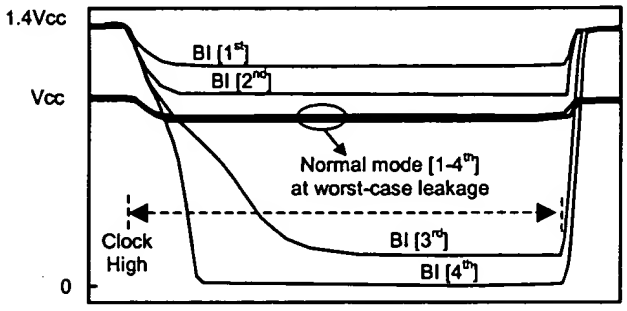

Fig. 8: Output voltage for the 4-stage domino circuit with standard keeper, at burn-in (BI) condition, and at normal operating condition for worst-case process leakage corners. Third stage has already collapsed at burn-in condition, while stable at normal-mode.

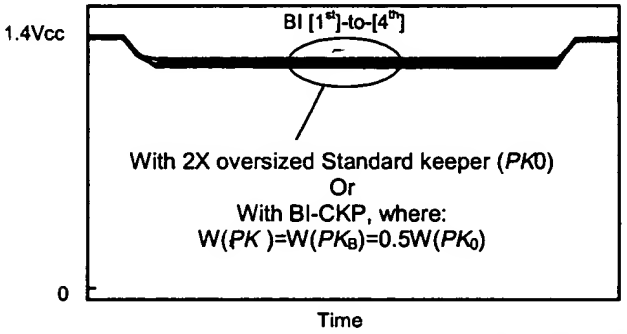

Fig. 9: Output voltage for the 4-stage domino circuit with 2X oversized standard keeper, at burn-in (BI) condition.

However, *BI-CKP* shows its advantage at normal operating mode (Fig. 10), where the 2X oversized standard keepers degrade the performance of the circuit significantly (20%), while *BI-CKP* shows 3% delay penalty only, resulting in 17% performance improvement over the oversized standard keepers.

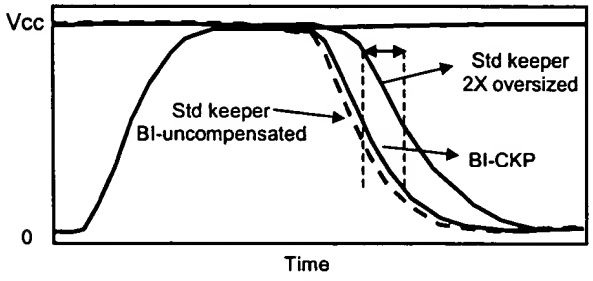

Fig. 10: Clock-to-output delay for the domino circuit utilizing burn-in uncompensated standard keeper, 2X oversized standard keeper, and BI-CKP.

We have also evaluated and compared the keeper in [8] (Fig. 6), with the proposed *BI-CKP* (Fig. 5). Table 1 shows that for the same burn-in robustness, *BI-CKP* results in ~62% transistor area saving, and ~30% smaller additional load on the output of the actual dynamic gate. For the 4-stage domino circuit with the 6-input *NOR*s (Fig. 10), the keeper in [8] results in ~7% larger delay penalty compared to the circuit with *BI-CKP*.

Burn-in Keepers	Total transistor width	Additional load at output
Keeper in [8]	1	1
BI-CKP	0.375	0.7

Table 1: Comparison result for the BI-CKP (Fig.5) vs. the previous work in [8] (Fig. 6).

Fig. 11 shows a more general comparison for the impact of keeper upsizing (for burn-in) on performance of the domino circuit. In contrast to the standard keeper, the delay is fairly insensitive to the size of *BI-CKP*. The figure also shows that the delay-penalty increases exponentially for larger standard keepers, and thus the benefit of *BI-CKP* is larger for larger keepers.

For the domino circuits with 2 and 4-input dynamic *NOR* gates using *BI-CKP*, the same level of burn-in robustness was achieved. However, at normal operating condition, *BI-CKP* results in larger performance improvement for wider gates with more number of parallel pull-down paths (Fig. 12). For wider gates the ratio between the weakest and strongest pull-down paths (input pattern dependant) is larger. Keepers have to be sized for the strongest pull-down, whereas the weakest pull-down path determines the performance (worst-case delay). Thus the weakest pull-down path experiences a stronger keeper. As a consequently, for the wider circuits with *BI-CKP* the downsizing of the normal-mode keeper leads to larger delay improvement.

The proposed *BI-CKP* is a general technique. The above test circuit was selected as an example to highlight the benefits. However, the advantageous properties of *BI-CKP* are independent of the topology of the dynamic gates, and we have observed similar conclusions for other dynamic circuits.

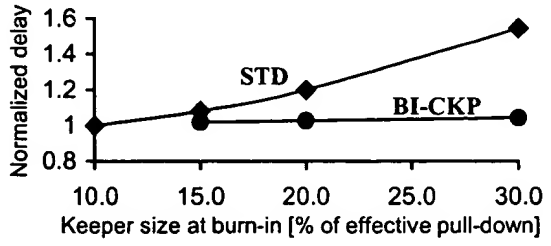

Fig. 11: The impact of keeper upsizing for burn-in on delay of the domino gate at normal operating condition.

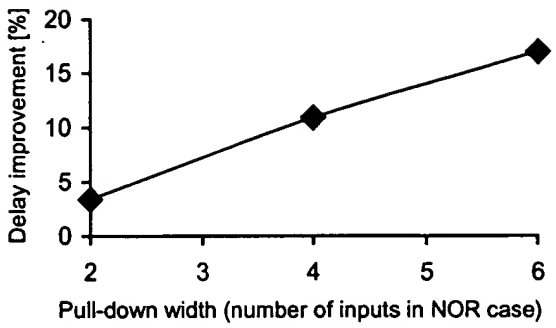

Fig. 12: The delay improvement, utilizing BI-CKP versus the oversized standard keeper for the 4-stage domino circuits using 2, 4, or 6-input NOR gates.

Conclusion

We have presented a general burn-in tolerant sub-130nm dynamic circuit technique, where the pre-charged gates utilize the proposed conditional burn-in keeper circuit, *BI-CKP*. Simulation results show that *BI-CKP* efficiently removes the conventional trade-off between robustness at burn-in versus performance of the gates at normal operating condition. The higher robustness of dynamic gates at burn-in allows the maximum burn-in temperature and voltage, and thus an efficient burn-in test, with the lowest burn-in cost. Further, compared to the previous work in [8], the proposed keeper topology results in 60% active area reduction, and ~30% lower extra load at the output of dynamic gates.

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